REMARKS

Claims 1-38 are pending in the present application.

Claims 1-38 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Liencres et al. (U.S. Patent No. 5,434,993) in view of Chandrasekaran et al. (U.S. Patent No. 6,970,872), and in further view of Roy (6,065,092). Applicant respectfully traverses this rejection.

Applicant's claim 1 recites a system comprising in pertinent part

> a node including an active device, an interface to an inter-node network, a system memory, and an address network and a data network that is separate from the address network, coupling the active device, the interface, and the memory;
>
> ...
>
> wherein in response to receiving **from the active device** an address packet initiating a transaction to gain an access right to a coherency unit, the **system memory** is configured to **send a report** corresponding to the address packet to the interface **if the transaction cannot be satisfied within the node**;
>
> wherein the interface is configured to ignore the address packet and to send a coherency message requesting the access right to the additional node via the inter-node network in response to the report. (Emphasis added)

The Examiner asserts the combination of Liencres and Chandrasekaran teaches all the limitations recited in Applicant's claim 1. Applicant respectfully disagrees with at least portions of the Examiner's assertions. More particularly, in response to the Examiner's response to arguments on page 2 of the instant Office action, Applicant submits the type of memory matters because of the topology of the system and the way in which a system memory is connected to the nodes, in contrast to how a cache memory is

connected. More particularly, Applicant was pointing out to the Examiner as shown in FIG. 3a, Liencres clearly shows that the memory alluded to by the Examiner is a cache memory 37, which is not coupled to the bus 33 but to the cache controller 35. Applicant understands the Examiner is allowed to interpret claims as broadly as is reasonably possible. However, Applicant believes the Examiner has overstepped reasonableness when comparing the topology of Liencres, and the system recited in Applicant's claim language.

The above notwithstanding, the Examiner acknowledges Liencres does not teach "wherein in response to receiving from the active device an address packet initiating a transaction to gain an access right to a coherency unit, the system memory is configured to send a report corresponding to the address packet to the interface if the transaction cannot be satisfied within the node."

The Examiner also asserts Liencres teaches ignoring the address packet, but acknowledges Liencres does not teach in response to the report, the interface sending "a coherency message requesting the access right to the additional node via the inter-node network," as recited in claim 1.

However, the Examiner asserts Chandrasekaran teaches the above limitations at col. 6 lines 25-36. The Examiner asserts "When another node writes out data, it sends out a report stating the latest write time for that data. The read data is invalid once its timestamp comes before the latest write time. The node, now having an invalid read data, will ignore the current address packet (col. 2, lines 60-66), and then have to request the updated data from the additional node. It would have been obvious… to employ optimistic reading of data using "write-time" validity checking so that reads could be employed when another node has exclusive access but hasn't yet written the data." Applicant respectfully disagrees with the Examiner's application of the Chandrasekaran art to Applicant's claims.

More particularly, Chandrasekaran is directed to optimistic reads and write time validity checking. Chandrasekaran discloses

> In an embodiment using the first type of validity checking, the time that the optimistic read is started is compared to the latest time that the data block was written by any of the other nodes. If the read was started after the last write, the read is valid. This can be determined even before the read is finished, but involves the writing node publishing its write time to the other nodes. A node can publish its write time in any way, such as by broadcasting the write time **to the other nodes**, by storing the write time and responding to requests **from other nodes**, or by **sending the write time to a lock manager**. This type of validity checking is called "write-time" validity checking herein. (See col. 6, lines 25-36) (Emphasis added)

> In step 210 a request for a lock to access a particular data block is sent. In embodiments that use a lock manager, the request is sent to the lock manager. In other embodiments, the lock manager may be omitted and the I/O processes **114** can communicate with each other to grant locks. In still other embodiments, other methods can be used to assure consistent content of a resource; and step 210 corresponds to initiating an operation to grant permission to access a resource in order to assure consistency of content of the resource. In some embodiments, a retrieval start time, indicating a time that step 220 is performed, is included in a message sent to a lock manager or the other nodes.
> In step 220, retrieval of the particular data block is started. For example, a call is made to an operating system function to move data from the disc data blocks corresponding to the particular data block into a location in the memory of one of the nodes. In some embodiments the location in memory is in the cache **112** for the I/O process **114** on the node; in some embodiments the location is a buffer outside the cache **112**. (See col. 7, lines 27-45) (Emphasis added)

> If it is determined in step 250 that the particular block returned in step 240 is not valid, then control passes to step 260. In step 260, the operation to retrieve the particular block from disk or a remote cache is started again, based on permission received in step 230. Because permission has been received in step 230 before performing step 260, the data block received in response to step 260 will be valid. In embodiments in which permission is not received in step 230, such as embodiments in which a message denying permission to access the particular data block is received in step 230, step 260 is delayed until permission is received. (See col. 8 lines 56-66) (Emphasis added)

From the foregoing description, Applicant submits Chandrasekaran is disclosing a given node broadcasting or somehow publishing its write time for a write of a given data block. That write time may be stored and then compared or it may be sent in response to a request for access. Some other node performs an optimistic read of the data, and if that read occurs earlier in time than the write, the read data would be invalid. The write time may be kept by **a lock manager** which returns the write validity information. Furthermore, Chandrasekaran is disclosing in response to a request for the data block, the data retrieval process is started irrespective of whether the data is valid (i.e., optimistically). Accordingly, the only way the data retrieval process can be started is if the data block is available. Now the data may not be valid due to the write time constraints, but it is still available, and the memory system does not have knowledge of that validity. This is in contrast to an active device within a given node requesting an access right to a coherency unit, and the system memory responding by sending a report (not the data) to an interface, if the transaction cannot be satisfied within the node. The interface ignores the address packet (since it came from within the node), but responds to the report by sending a coherency message out to the other nodes. This is clearly not taught or suggested by Chandrasekaran.

Roy is not relied upon nor does Roy teach the above limitations.

From the foregoing, Applicant submits none of the cited references taken either singly or in combination teach or suggest the combination of features recited in Applicant's claim 1. Accordingly, Applicant submits claim 1, along with its dependent claims patentably distinguishes over Liencres in view of Chandrasekaran in view of Roy for the reasons given above.

Applicant's independent claims 14 and 26 recite features that are similar to the features recited in claim 1. Thus Applicant submits claims 14 and 26, along with their respective dependent claims, patentably distinguish over Liencres in view of Chandrasekaran in view of Roy for at least the reasons given above.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-01601/SJC.

Respectfully submitted,

/ Stephen J. Curran /
Stephen J. Curran
Reg. No. 50,664
AGENT FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800

Date: February 26, 2008